REQUEST FOR APPLICATIONS
DOWNSTATE SEMICONDUCTOR CHIP DESIGN CENTER

Addendum #1

Webinar

The information session was held on September 17th, 2026, at 1pm via Zoom and lasted approximately one hour.

A copy of the presentation of the Downstate Semiconductor Chip Design Center Webinar is available below:

DOWNSTATE SEMICONDUCTOR CHIP DESIGN CENTER WEBINAR

REQUEST FOR APPLICATIONS

Presented by

GO-SEMI
GOVERNOR'S OFFICE OF SEMICONDUCTOR EXPANSION, MANAGEMENT, AND INTEGRATION

Procurement

All contacts/inquiries/questions shall be made by email to the following address: DownstateSemiconductorChipDesign2026@esd.ny.gov

All questions should be made September 22, 2026. Answers will be posted no later than October 2, 2026. Additionally, please monitor the official websites for all updates.

- NYS Contract Reporter
- The Empire State Development website

Designated Contacts for this Procurement:

- Primary Contact: Shanah Jack
- Secondary Contact: Ralph Volcy

Project Summary

- Global semiconductor revenues are projected to approach $1 trillion by the end of 2026, underscoring the industry’s growing economic and strategic importance.

- Since 2022, semiconductor companies have announced over $124 billion in new investments across upstate New York, cementing the State's position as a global leader in semiconductor manufacturing and innovation.

- Despite New York's strengths in R&D and manufacturing, chip design remains a critical gap in the State's semiconductor ecosystem. The U.S. private sector is projected to commit up to $500 billion over the next ten years in semiconductor design-related investments.

- Strengthening New York's chip design sector ensures semiconductor breakthroughs are both conceived and produced locally.

Schedule

Item	Date
Release of Request for Applications	On or about September 10, 2026
Webinar*	September 17, 2026, at 12:00 PM
Deadline for Submission of Questions	September 22, 2026
Deadline for ESD to Respond to Questions	On or about October 2, 2026
Application Submission **Phase 1 – Concept Paper**	October 26, 2026, by 2:00 PM EST
Phase 2 – Interactive Review Process	On or about November 9 - 20, 2026
Phase 3 – Full Proposals Due	January 11, 2027
Anticipated Selection	February 2027
Anticipated Contract Start Date	July 2027

Project

Under this RFA, ESD anticipates selecting one qualified organization to lead the design, construction, development and operation of a world-class Semiconductor Chip Design Center.

Downstate, in the context of this RFA, shall refer to:

- The five boroughs of New York City
- Westchester, Rockland, Putnam, Dutchess, Orange Nassau and Suffolk Counties

The creation of the Center may involve multiple partners and could be a new building and/or the expansion or modification of an existing structure.

The Center will leverage downstate New York's dense tech sector and knowledge economy—universities, research institutions, startups, venture capital, and private-sector partners—to complement the State's established upstate manufacturing and R&D assets.

Project Goals and Objectives

Center Establishment

Build and manage a physical semiconductor chip design center in downstate New York. Establish a sustainable operating model that leverages State support alongside industry, academic, and philanthropic partnerships.

Access to Advanced Tools

Provide shared access to industry-standard electronic design automation (EDA) tools, computing resources, and secure design environments to reduce barriers to market entry for early-stage firms and academic teams.

Prototyping & Validation

Support innovation in early-stage chip design, including architecture development, design verification, and pre-manufacturing validation, connecting design efforts with manufacturing and prototyping resources.

Startup Incubation

Incubate and/or accelerate chip design and related semiconductor startups by providing access to design tools, guidance on intellectual property strategy, commercialization pathways, and connections to investors and strategic partners.

Workforce Pipeline

Deliver training programs that prepare New York residents for high-skill chip design roles, including upskilling and/or reskilling opportunities.

Performance Measurement

Establish metrics to track outcomes, including number of startups supported, designs advanced, and partnerships formed. Provide regular reporting to New York State on progress, challenges, and impact.

Eligibility Requirements

To be eligible to receive grant proceeds from ESD, an applicant must meet the following minimum qualifications:

Good Standing: Applicant must be in good standing with the State of New York and Empire State Development (ESD).

Nonprofit Status: Must be a 501(c)(3) nonprofit organization, including academic or research institutions.

Consortia Applications: Consortia comprised of two or more eligible entities may apply. Any consortia application must have one lead Applicant who, if awarded, will act as the fiscal agent and will be responsible for all contractual obligations with ESD.

Eligible and Illegible Expenses

A grant of up to $25 million is available for capital costs to support the creation and development of the Center. ESD reserves the right to award grants in amounts greater or less than the listed figures and/or at a varying schedule depending on the number and quality of applications received. **There is no cost-match requirement associated with this grant.**

Eligible Capital Costs

- New construction, renovation or leasehold improvements
- Machinery and/or equipment
- Demolition and environmental remediation
- Furniture and fixtures
- Soft costs of up to twenty-five percent (25%) of costs related to the eligible capital expenditures
- Other costs and expenditures deemed eligible by ESD

Ineligible Expenses

- Developer fees
- In-kind costs
- Overhead and indirect costs, including but not limited to
    - o Salaries and wages
    - o Rent/lease costs
    - o Marketing or advertising media costs
- Costs associated with completing an application
- Other costs / expenditures deemed ineligible by ESD

Application Process

ESD intends to conduct this application process through a progressive, multiphase competitive selection process. The approach is designed to:

- encourage innovative concepts
- reduce proposal development costs for applicants
- facilitate meaningful dialogue between ESD and applicants
- evaluate organizational readiness, leadership, facilities, and partnerships
- strengthen full proposals through constructive feedback prior to final submission

Phase 1 – Concept Paper

The purpose of Phase 1 is to evaluate strategic merit and overall competitiveness of each proposed Center. The concept paper should not exceed ten pages and should emphasize strategic approach, rather than detailed implementation plans across the following areas:

- Value Proposition to Industry and to NYS: Understanding of the industry demands/challenges and the addressable market needs to be served by the proposer's downstate chip design center.

- Team: Consortia composition and proposal partners

- The Project: Description and location of center facilities

- The Impact: Vision and mission for providing barrier-free access to advanced chip design tools and resources to students, career explorers, innovators and entrepreneurs.

- The Proposal: Win Themes for the proposal

Phase 2 – Interactive Review Process

Selected proposal teams may be invited to participate in an interactive review process. The purpose of this phase is to allow ESD to better understand each proposed Center and to provide proposers with an opportunity to clarify, refine, and strengthen their proposed approach prior to the submission of a full proposal. The interactive review process may include some or all of the following:

- In-person executive presentation
- Question and answer session
- Leadership interview
- Consortia partner discussion
- Governance discussion
- Financial discussions
- Facility tours
- Meetings with lead applicant leadership
- Meetings with industry partners
- Meetings with workforce and startup/innovation partner

Phase 3 – Submit Full Proposal

Following the completion of Phase 2, ESD may invite one or more interactive finalists to submit a full proposal. The full proposal shall present a comprehensive implementation plan that incorporates, where appropriate, information exchanged during the interactive review process.

Executive Summary (1 page)

Proposal (30 page minimum)

- Center Establishment and Operations
- Industry Expertise and Partnerships
- Access to Advanced Chip Design Tools and Infrastructure
- Startup Incubation and Workforce Development
- Budget – Capital and Operations
- Timeline

Review Criteria

The section for award will be based on best value to ESD and will consider factors including but not limited to:

1. Ability to Perform
   - Experience of the Applicant Institution and the staff proposed to execute the Application Scope of Work.
   - How well the organization meets the qualification requirements addressed in this RFA.
   - Access to data and resources to accomplish the Application Scope of Work.
2. Knowledge of Advanced Industry Sectors
   - Knowledge, experience and skills of the organization and the staff proposed to undertake advanced industry sector studies.
3. Project Readiness and Workplan
   - Overall work/action plan.
   - Measurable deliverables and completion dates.
4. Use of Funds
   - Quality of the applicant institution's justification/rationale for the use of the requested funds.
5. Proposal Clarity
   - Quality of proposal's organization, clarity and adherence to page limitations.
6. References
   - Quality of references that can substantiate the quality of the Bidder's work to be considered for an award of this project.

Submission and Questions

Questions
All questions, comments, requests for clarification or any other communication regarding this RFA must be submitted by email to DownstateSemiconductorChipDesign2026@esd.ny.gov no later than September 22, 2026.

Your subject line should state: “[Name of Applicant] – RFA Inquiry, Downstate Design Center”.

Submission
All applications should be submitted via email to DownstateSemiconductorChipDesign2026@esd.ny.gov no later than October 26, 2026, 4:00 PM EST.

Applicant subject line should state: “[Name of Applicant] – RFA, Downstate Design Center”.

Award Terms & Disbursement Conditions

Contingent Grant Agreement: Selection through this solicitation does not constitute an award of grant funding and does not create any entitlement to receive State financial assistance. Any grant awarded shall be contingent upon availability of funds, and subject to all applicable State laws, regulations, ESD policies, and required approvals.

Reimbursement Basis: Unless otherwise approved by ESD, grant funds shall be disbursed on a reimbursement basis for eligible project costs incurred in accordance with the executed Grant Disbursement Agreement.

5-Year Recapture & Reports: Recapture terms will apply for five years authorizing ESD to reduce, withhold, or recover grant funds in whole or in part if the recipient fails to satisfy material program requirements, contractual obligations, or approved performance commitments.

Procurement Requirements

Additional requirements for this RFA are listed below. Relevant forms, where required to be submitted, must be executed and included in the submission in the same order as listed below:

1. Conflict of Interest
2. 139 J&K
3. Vendor Responsibility Questionnaire
4. Compliance with State Finance Law Section 139-m
5. Insurance Requirements
6. Non-Discrimination and Contractor & Supplier Diversity Requirements
7. W-9

Thank You

Presented by